ABSTRACT OF THE DISCLOSURE

An EEPROM cell with reduced cell size and improved circuit performance includes a high-voltage (HV) capacitor, a low-voltage(LV) read path, and an HV write path, wherein either the HV capacitor is placed between the LV read path and the HV write path or the HV write path is placed between the LV read path and the HV capacitor. The EEPROM cell also includes a native floating-gate (FG) transistor in the LV read path. Using a native FG transistor in the LV read path results in further reduction in the cell size and improved circuit performance of the EEPROM cell.